REMARKS

Applicants respectfully request reconsideration of the present application and allowance of pending claims 1-5, 8-11, 13, 14, 16-18, and 20-28.

Amendments to the Specification

In this response, Applicants have amended the specification to improve its readability. These changes do not add any new matter.

Objections to the Claims

The Examiner has objected to claims 21 and 27 because of some informalities. In particular, the Examiner requested that the terms "first and second" in claims 21 and 27 be changed to the terms "input and output."

By this response, Applicants have made these changes requested by the Examiner. Based on these claim amendments, Applicants respectfully request that the Examiner withdraw the objection to the claims 21 and 27.

Double Patenting

The Examiner has objected to claim 18 as being a substantial duplicate of claim 16.

By this response Applicants have amended claim 18 to depend from claim 17, while claim 16 remains dependent upon claim 9.

As a result of this amendment, claim 18 is no longer a substantial duplicate of claim 16. Applicants therefore respectfully request that the Examiner withdraw the objection to claim 18.

Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 1, 8, 20, 22, and 26 under 35 U.S.C. § 102(b) as being allegedly anticipated by United States Patent No. 6,201,674 to Warita et al. ("Warita").

By this response Applicants have amended claim 8 to depend from claim 3, which the Examiner has indicated is allowable. Similarly, Applicants have amended claim 20 to depend from claim 2, which the Examiner has also indicated is allowable.

Since claims 8 and 20 both now depend from an allowable claim, Applicants respectfully submit that they are also allowable, and that this rejection is moot as it pertains to claims 8 and 20.

Regarding claims 1 and 22, claim 1 recites "a limited-current-value setting circuit setting a limited value to the output current, the limited value increasing gradually over time during a rise of the output voltage up to the target voltage," and "a current limiting circuit controlling the electric switching element to keep the detected output current at a current value less than or equal to the limited value during the rise of the output voltage up to the target voltage, the current limiting control having priority over an output voltage tracking control." Similarly, claim 22 recites "a limited-current-value setting circuit setting a limited value to the output current when a predetermined delay time has passed from an application of the input voltage to the input terminal, wherein the limited value increases gradually with a progress in time during a rise of the output voltage up to the target voltage," and "a current limiting circuit controlling the switching element to keep the detected output current at a current value less than or equal to the limited value during the rise of the output voltage up to the target voltage, the current limiting control having priority over an output voltage tracking control."

In each of claims 1 and 22, the recited limited-current-value setting circuit sets a limited value that increases gradually over time during the rise of the of the output voltage to a target voltage. A current limiting circuit then controls an electric switching element to keep its detected output current at a current value less than or equal to the limited value. This is shown in Applicants' specification and drawings, by way of example, in elements 21, 22, and Q13 of FIGs. 2 and 3.

The limited value recited in claims 1 and 22 represents a current value over which a detected output current value should not rise over time. This is seen in the limited-current-value setting circuit 21 of FIG. 3, which produces a reference voltage that corresponds to a limit value to the output current Io, between the terminals across a resistor R15 connected to both the IC terminal 15c and the non-inverting input terminal of the operational amplifier 22. (See, e.g., Applicants' specification, page 10, lines 27-31, and FIG. 3.) The limited value (i.e., the reference voltage VP output from the limited-current-value setting circuit 21) rises based on the value of the reference current I1 flowing through the resistor R15. But this reference current changes over time, depending upon which of the reference current generating circuits 28a, 28b, 28c, and 28d are turned on. As the timer circuits 30a, 30b, 30c, and 30d operate after a start time t0, more of the reference current generating circuits 28a, 28b, 28c, and 28d will turn on, thus raising the reference current I1 and with it the limited value VP.

The operational amplifier 22 then compares the values of VP (received from the limited-current-value setting circuit 21) and VM (received from the IC node 15d) to determine whether to turn the transistor Q13 on or off, thus turning off the transistors Q12 and Q11, limiting the current passing between the input terminal 12 and the output terminal 13. This allows the output current Io to be controlled in a stepwise manner, which can reduce an overshoot of the output voltage Vo.

In contrast, the Examiner has asserted that Watari shows the recited limited-current-value setting circuit in the error amplifier 18, and shows the recited current limiting circuit in the transistor Q10. However, a careful examination of Watari will show that this is not the case.

The error amplifier 18 of Watari compares a between-terminal voltage Vs with reference voltage Vres2, and outputs a signal that controls the conduction of the transistor Q10. But even if the output of the error amplifier rises slightly over time, this is still not the same as setting a limited value to the output current, the limited value increasing gradually over time. The output of the error amplifier 18 does not represent a limit to the output current Io in Watari.

The transistor Q10 operates in response to the signal from the error amplifier 18. When it is rendered conductive, it bypasses the control current to transistor Q12 so as to suppress the base current Id. But this does not "keep the detected output current at a current value less than or equal to the limited value," as required by claims 1 and 22. The Examiner appears to assert that the recited "limited value" in Watari is the output voltage of the error amplifier 18. But the output of the error amplifier 18 does not represent a limit for the output current Io.

In operation the error amplifier 18 compares the between-terminal voltage Vs with the reference voltage Vres2, and when the between-terminal voltage Vs exceeds the reference voltage Vres2, it outputs a signal that renders the transistor Q10 conductive. But this is a constant comparison. In no way is the limit of the output current Io connected to the output voltage of the error amplifier 18.

In fact, an object in Watari is to finely control an over-current flow when a short-circuit event occurs or a high-amount load is connected. To realize such an object, the output current is decreased as the output voltage decrease. A decrease in this output current will lead to saving the power consumed by the external transistor TR in FIG. 1. But such a teaching does not disclose or suggest "a limited-current-value setting circuit setting a limited value to the output current, the limited value increasing gradually over time during a rise of the output voltage up to the target voltage," as recited in claims 1 and 22.

Claim 26 depends from claim 22 and is allowable for at least the reasons given above for claim 22.

Thus, Watari does not disclose every feature recited in claims 1 and 22. Based on at least the arguments given above, Applicants therefore respectfully request that the Examiner withdraw the rejection of claims 1, 8, 20, 22, and 26 under 35 U.S.C. § 102(b) as being allegedly anticipated by Warita.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 21, 27, and 28 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Warita in view of Applicants' FIG 1.

By this response Applicants have amended claim 21 to depend from claim 2, which the Examiner has indicated is allowable. Since claim 21 now depends from an allowable claim, Applicants respectfully submit that it is allowable and that this rejection is moot as it pertains to claim 21.

Claims 27 and 28 depend from claim 22 and are allowable for at least the reasons given above for claim 22. What Warita fails to disclose, it also does not suggest. And nothing in Applicants' FIG 1 cures the deficiencies in Warita discussed above.

Based on at least the arguments given above, Applicants therefore respectfully request that the Examiner withdraw the rejection of claims 21, 27, and 28 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Warita in view of Applicants' FIG 1.

Claim Amendments

Applicants have amended claims 1 and 27 to better recite the claimed invention. In particular, claim 1 is amended to recite that "the limited value increasing gradually" rather than "wherein the limited value increases gradually," and claim 27 is amended to correct a typographical error and change "he" to "The." These additional amendments to claims 1 and 27 are being made solely to improve their readability and should not be considered as limiting the application of the doctrine of equivalents on these claims.

Allowable Subject Matter

The Examiner has objected to claims 2-5, 9-11, 13, 14, 16-18, and 23-25 as being dependent upon a rejected base claim, but has indicated that they would be allowable if rewritten into independent form including all of the limitations of the base claim and any intervening claims.

By this response Applicants have amended claims 2, 9, and 23 into independent form. Claims 2 and 9 have been amended to incorporate the limitations of claim 1, from which they depend, and claim 23 has been amended to incorporate the limitations of claim 22. Claims 3-5 depend from claim 2 and are allowable for at least the reasons as claim 2. Claims 10, 11, 13, 14, and 16-18 all ultimately depend from claim 9 and are allowable for at least the reasons as claim 9.

Based on these amendments, claims 2-5, 9-11, 13, 14, 16-18, and 23 are now in a condition that the Examiner has indicated would be allowable.

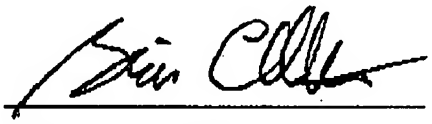
Claim 24 has been amended to depend from claim 22, and claim 25 depends from claim 24. Claim 22 is allowable for at least the reasons given above. Therefore, Applicants respectfully submit that claims 24 and 25 are also allowable.

Conclusion

In view of the foregoing, Applicants respectfully submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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Date: September 24, 2005

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